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A Low Power Radix-4 Adder Using Domino Logic

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Abstract:
Reduction of computational costs can be achieved effectively by approximate computing. With this approach, the circuit's power use, latency, and area are traded off against computational precision. For various applications, the accuracy requirements could change, never the less. In some circumstances, precise outcomes are necessary. In order to compute accurate or approximate results, we used the construction of the radix-4 adder using domino logic. As we take reference circuit of radix-4 adder with 2 2 bit adders are to be added. This circuit includes the combination of AND gates, OR gates, NOR gates and XOR gates. This reference circuit has three outputs and five inputs. Also, this circuit has a good power reduction capability, but by using the domino logic we can reduce even more power consumption in the circuit. In this the domino logic is implemented to the one path of the reference circuit by using the domino logic. So, we can get the same output with a better power reduction process. As we compared the both circuits, the area and the power consumption was greatly reduces in the domino logic implemented circuit

Key Word*: Domino Logic, Radix 4 Adder, Approximate Computing, Computational costs, Precision.*

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I. Introduction

Power consumption and performance are the two primary issues these applications face when developing their circuits. However, due to the limitations of human eyesight, even inaccurate calculations can lead to beneficial results for individuals. In the field of digital circuits and computer arithmetic, adders are essential building blocks used to perform arithmetic operations on binary numbers. The traditional radix-2 adder is widely used in most digital systems, but it has limitations in terms of speed and efficiency. This has led to the development of more advanced adder architectures, such as the radix-4 adder. The radix-4 adder is a digital circuit that performs binary addition using a radix-4 number system, which allows for more efficient computation than traditional radix-2 systems. It achieves this by breaking down the input binary numbers into groups of four bits and performing addition on each group separately. The individual group additions are then combined using carry-select adder stages to produce the final sum. The use of a radix-4 number system in the design of the adder offers several advantages over the traditional radix-2 system. For example, it allows for four possible values per digit, which reduces the number of digits required to represent a given number, leading to fewer logic gates needed to perform addition. This results in shorter propagation delays and faster overall computation times. However, the increased complexity of the radix-4 adder, which requires additional circuitry, can be a drawback.

II. Existing Method

The Existing method of the project has five inputs along with carry input and a set of two inputs of Ai+1, Bi+1, Ai, Bi and Cin. This existing method is known as Conventional Radix 4 Adder. This also consists of three outputs of carry out, Sumi+1 and Sumi. This is the simple adder which consists of AND Gate, OR Gate, NOR Gate, XOR Gate and an inverter. As these are connected with a specific time slots and according to the specific algorithmic equation the circuit is connected. Then the functioning of the Conventional Adder circuit is as there are five inputs connected to the specific logic gates as shown in the figure. The logical equation of above figure is as follows

$$\mathbf{C_{out} = A_{i+1}B_{i+1} + (A_iB_i)(A_{i+1} + B_{i+1}) + C_{in}((A_i + B_i)\,(A_{i+1}+ B_{i+1}))}$$

$$\mathbf{Sum_{i+1} = (A_{i+1} \oplus B_{i+1}) \oplus (A_iB_i + C_{in}A_i + C_{in}B_i)}$$

$$Sum_i = (A_i \oplus B_i) \oplus C_{in}$$

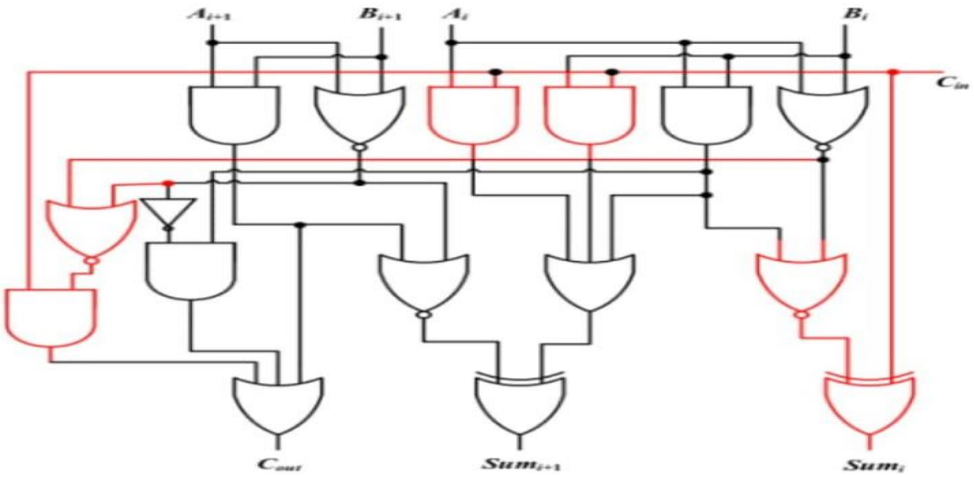

Figure No 1: Circuit diagram of Radix 4 Adder

III. Proposed Method

Introduction to Domino Logic

Domino logic is one of the most effective circuit configurations for implementing high speed logic designs. Domino circuits offer the advantages of faster transitions and glitch-free operation. Domino logic is a CMOS-based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors. It runs 1.5-2 times faster than static CMOS logic because dynamic gates present much lower input capacitance for the same output current and a lower switching threshold. In Domino logic a single clock is used to precharge and evaluate a cascaded set of dynamic logic blocks

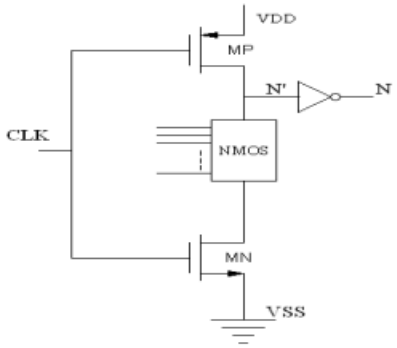

FIGURE 2: Domino Logic

Radix 4 Adder Using Domino Logic

In digital circuits, adders are important components used to perform arithmetic operations on binary numbers. Radix-4 adders are a type of adder that can add four binary digits in parallel. However, the traditional carry path used in radix-4 adders can limit the speed and power efficiency of the circuit. In this matter, we will discuss how the carry path of a radix-4 adder can be replaced with domino logic to improve its performance. Domino logic is a type of dynamic logic that uses precharged nodes and pass-transistor logic to reduce the delay in the circuit. In domino logic, the precharge phase charges the nodes to a pre-defined voltage level, and the evaluate phase switches the nodes based on the input signals. This technique allows for faster switching times and lower power consumption compared to traditional static CMOS logic.

Replacing the carry path of a radix-4 adder with domino logic involves modifying the internal structure of the adder. In the traditional radix-4 adder, the carry path consists of a series of full adders that propagate the carry from one stage to the next. In the modified adder, the full adders are replaced with domino logic gates that perform the same function. Specifically, each full adder is replaced with a domino adder that uses precharged nodes and pass-transistor logic to propagate the carry signal. The domino adder consists of two stages, the precharge stage and the evaluate stage. In the precharge stage, the internal nodes of the adder are precharged to a

high voltage level. The inputs to the adder are then applied during the evaluate stage, causing the nodes to switch based on the input signals. The output of the domino adder is then latched using a traditional static CMOS latch to ensure that it maintains its value until the next clock cycle. Replacing the carry path of a radix-4 adder with domino logic can provide several benefits. First, the use of dynamic logic can reduce the delay in the carry path, improving the overall speed of the adder. Second, the precharged nodes and pass-transistor logic used in domino logic can reduce power consumption, making the adder more energy-efficient. Finally, the smaller size of the domino logic gates can reduce the area of the adder, making it more compact and easier to integrate into larger circuits.

IV. Result

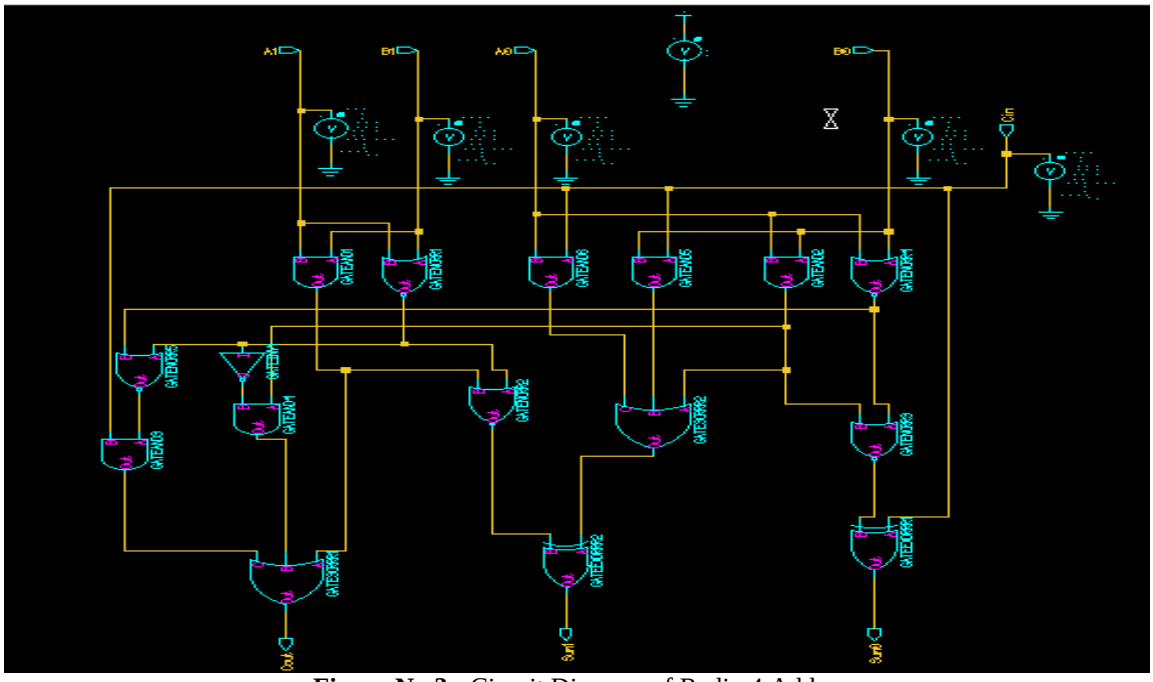

Figure No 3 : Circuit Diagram of Radix 4 Adder

Figure No 3 shows the existing circuit of radix-4 adder which is a combination of AND, OR,NOR, XOR and Inverter of Static CMOS logic gates. In this circuit the logic gates are connected with a five inputs which are Ai+1, Ai, Bi+1, Bi and CIN with the outputs of COUT, SUMi+1,SUMi. The above circuit consumes the power of 1.6838UWatts. The number of transistors present in the circuit is 98 with the time delay of 149.96ns.

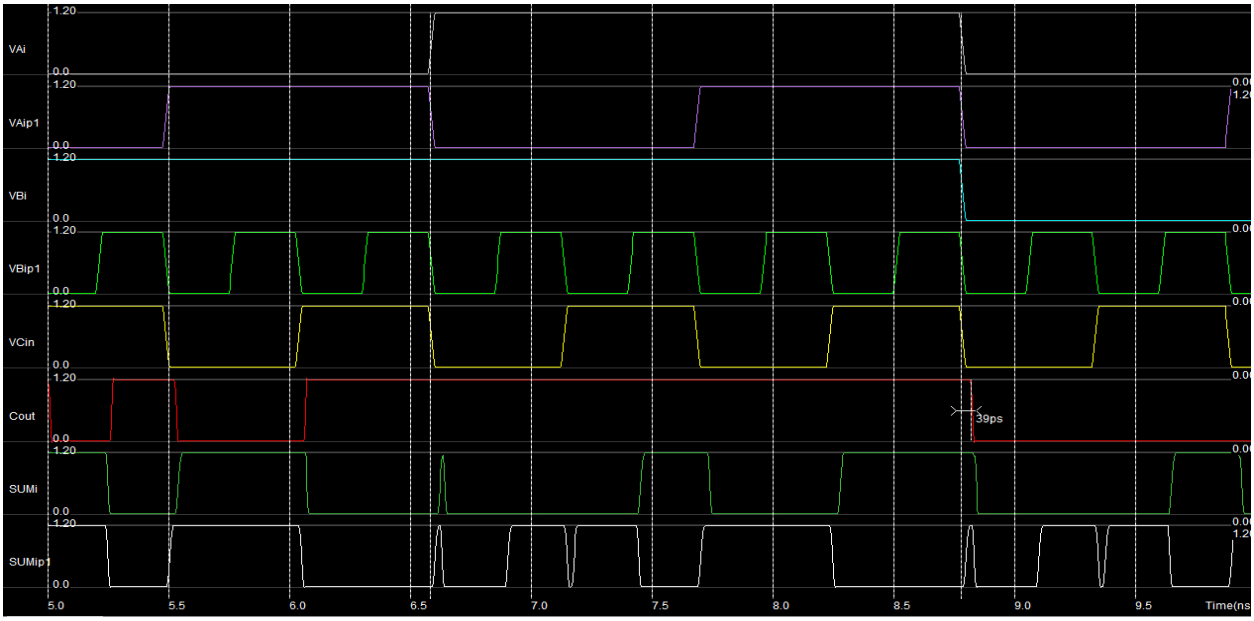

Figure No 4 : Waveforms of Radix 4 Adder

Figure No 4 shows the output waveforms of the radix -4 adder which is the existing adder of the project. This contains five inputs and three outputs. These waveforms are generated in the Mentor Graphic Software. In this circuit the logic gates are connected with a five inputs which are Ai+1, Ai, Bi+1, Bi and CIN with the outputs of COUT, SUMi+1,SUMi.

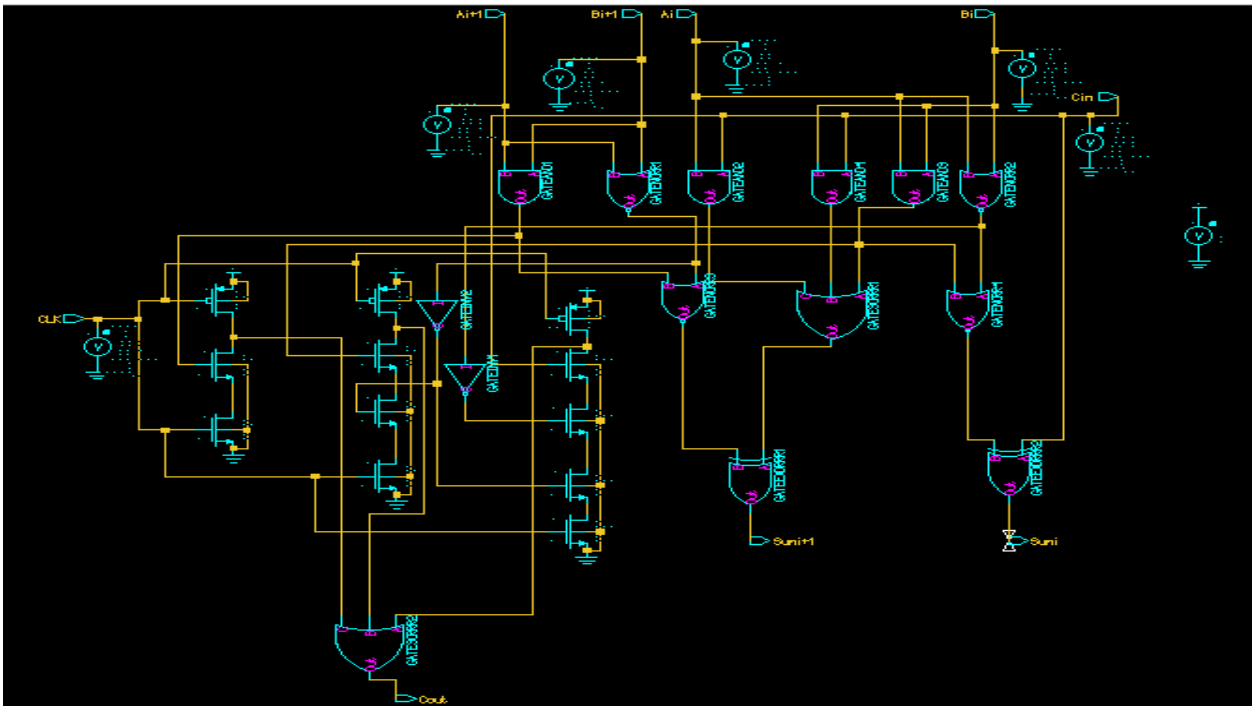

Figure No 5: Circuit Diagram of Radix 4 Adder Using Domino logic

The Figure No 5 shows the circuit diagram of radix-4 Adder which is proposed method using domino logic. In this circuit the logic gates are connected with a five inputs which are Ai+1, Ai, Bi+1, Bi, CIN and CLK with the outputs of COUT, SUMi+1,SUMi. In this circuit some part of the circuit is modified with domino logic as shown in the left side of the circuit. The domino logic is done by using the logarithmic equation of the COUT. By that the power consumption by the circuit is greatly reduced. The power consumed by the above circuit is 1.1000UWatts. The number of transistors present in the circuit is reduced by 9 CMOS transistors. The number of transistors present in the circuit is 89 with the time delay of 99.827ns.

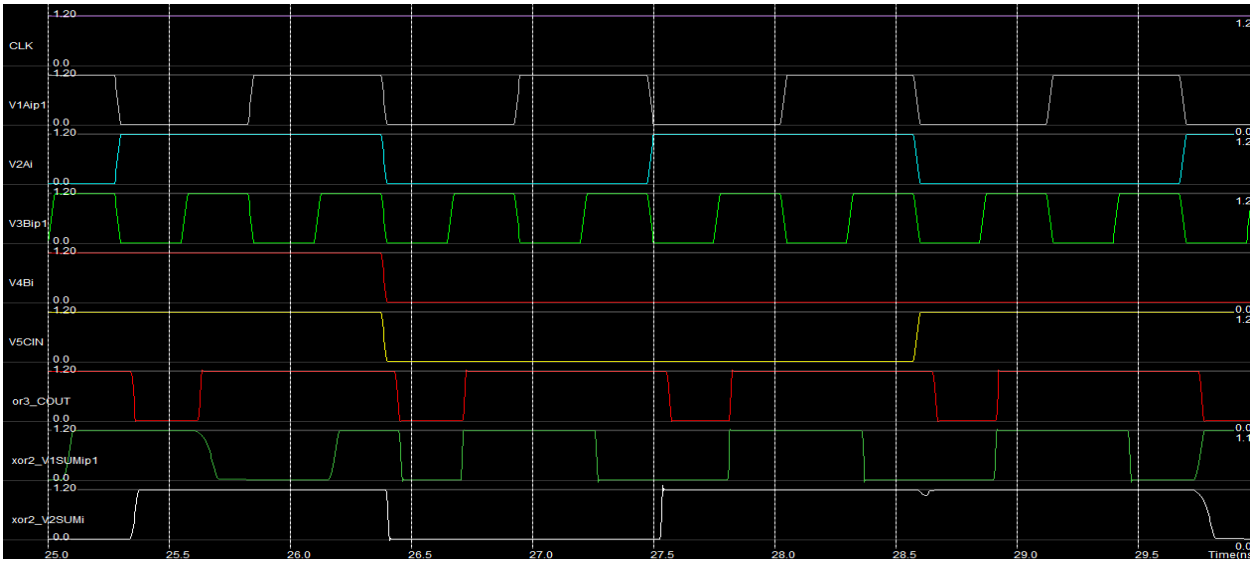

Figure No 6 : Waveforms of Radix 4 Adder using Domino logic

The above figure is the waveform or the result of radix-4 Adder which is a proposed method using domino logic. In this circuit the logic gates are connected with a five inputs which are Ai+1, Ai, Bi+1, Bi, CIN and CLK with the outputs of COUT, SUMi+1,SUMi. The waveforms are generated as same as the existing adder but in this there is an extra input which is clock given to the domino logic which is a crucial input to the circuit and decides the way of outputs in the waveform.

Comparison:

Table No 1: Power comparison of Existing and Designed Adders

ADDER	POWER
Radix-4 Adder	1.6838UWatts
Radix-4 Adder using DOMINO LOGIC	1.1000UWatts

Table No 1 shows the power comparison between the existing adder and the modified radix 4 adder using domino logic. In that the power consumed by the conventional radix 4 adder consumes the power of 1.6838UWatts. The modified radix 4 adder using domino logic consumes the power of 1.1000UWatts. By that the modified adder reduces the power by 33% than the conventional radix 4 adder.

Table No 2: Transistor Comparison of Existing and Designed circuit

ADDER	NUMBER OF TRANSISTORS
Radix-4 Adder	98
Radix-4 Adder using DOMINO LOGIC	89

Table No 2 shows the transistor comparison between the existing adder and the modified radix 4 adder using domino logic. In that the number of transistors used by the conventional radix 4 adder is 98 and the number of transistors used by the designed adder is 89. Therefore 9 transistors are reduced in the designed circuit. So that the area of the circuit is also reduced.

Table No 3: Delay Comparison of Existing and Designed Circuit

ADDER	DELAY
Radix-4 Adder	149.96ns
Radix-4 Adder using DOMINO LOGIC	99.827ns

Table No 3 shows the delay comparison between the existing adder and the modified radix 4 adder using domino logic. In that the time delay for the radix 4 adder is 149.96ns and the time delay for the radix 4 adder using the domino logic has the time delay of 99.827ns. So that the delay is reduced in the designed circuit.

V. Conclusion

In this both circuits are constructed and compared the parameters of power, area and number of transistors of the circuit. The existing method is designed by using static CMOS gates has 98 CMOS transistors in the circuit with the power consumption of 1.6838UWatts. The proposed method of Radix-4 Adder using Domino logic uses 89 CMOS transistors with a power consumption of 1.1000UWatts. By using the domino logic in the radix-4 adder the number of transistors are reduced by 9 and the power consumption is reduced by 65%. The reference circuit has the delay of 149.96ns and the domino logic used adder has the delay of 99.827ns which is more accurate than the existing circuit by 66%.

In future by using adiabatic logic, Power gating technique and Error correction techniques are used to reduce even more power consumption, area in the circuit.

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